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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/939,870 | 08/27/2001 | Yoko Hayashida | N26180400W | 4837 |

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| EXAMINER | |
|---|---|
| NGUYEN, DANNY | |
| ART UNIT | PAPER NUMBER |
| 2836 | |

DATE MAILED: 10/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/939,870 | Applicant(s) HAYASHIDA ET AL. |
|---|---|---|
| | Examiner Danny Nguyen | Art Unit 2836 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Drawings*

1. Figures 15-19 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claims 1-20 are objected to because of the following informalities:

Claims 1 and 16, p. 28 and 32, lines 2, an insulated gate field effect transistors "(IGFETs)" should be read "IGFETs". Appropriate correction is required.

Claims 2-19 are objected because they depend on claims 1 and 16.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 16-18 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art (APA).

Regarding to claim 16, APA discloses that a method for designing a semiconductor integrated circuit device including IGFET (see fig. 15) comprises executing a simulation with a predetermined charged device model (CDM) circuit that includes a first clamping device (111) connected to an I/O terminal (110), a first IGFET (112) having a gate connected to the I/O terminal through a first resistance (R114), a second clamping device (113) connected between gate and source/drain terminals of the first IGFET and connected to a supply potential wiring (117), the first and second clamping devices being connected to one another through a second resistance (116), and select a ratio of the second resistance and the first resistance to prevent potential between the gate and source/drain terminal of the first IGFET from exceeding a predermined value (see back ground of invention, p.5,6, lines 16-5).

Regarding to claims 17 and 18, APA discloses that the method of the predetermined value is determined from a relationship between CDM test results and the ratio of the second resistance (see fig. 16) and the first resistance (R114), and simulation test results showing a relationship between a potential between the gate and the source/ drain of the first IGFET (112) and ratios of the second resistance and the first resistance.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Taillient (USPN 5,515,226).

Regarding to claims 1, 3,15, APA discloses that an apparatus for a semiconductor integrated circuit device (see fig. 18) comprises a plurality of transistors (112a to 112c) coupled to a corresponding I/O terminal (110a to 110c) through a corresponding first resistance (Rin is (R114) inherent in the semiconductor device, as shown in fig. 15); a first clamping device (111a) coupled to each I/O terminal (110a); a second clamping circuit corresponding to each transistor, each second clamping circuit including a second clamping device (113a) and the corresponding the first resistance, each second clamping device having a first terminal connected to the gate of the corresponding transistor (112a) and a second terminal connected to a source/drain of the corresponding transistor and a supply potential wiring (118); each first clamping device being coupled to one second clamping device through a second resistance (114a). APA does not disclose that at least two of the second clamping devices are different.Taillient discloses that a second limiter (EC2j) of semiconductor integrated circuit device (fig. 4C) can be varied depending on the location of the transistor. Taillient discloses the second limiter (EC2j) of transistor (ELj) can be varied depending on the protection level needed by he transistor (ELj) due to its location relative to the pad which it is connected to (see col. 3, lines 15-19). Therefore, it would have been obvious to one having ordinary skill in the art at

the time invention was made to utilize the teaching of Taillient in order to vary the second clamping circuit of APA in order to provide the protection as needed by the individual transistor depending on its location and protected level needed.

Regarding to claim 2, APA discloses that a supply potential wiring is selected from the group of consisting of an electric power supply potential wiring (118), and a ground electric potential wiring, and a substrate electric potential wiring (117) (see p. 3, lines 2-3).

Regarding to claims 4, APA discloses that the two second clamping devices vary by a first resistance (Rin) of one second clamping circuit (113a) having a different value than the first resistance (Rin) of other second clamping device (113b) and the ratio between the first resistance and the second resistance having a predetermined value, and the predetermined value is determined from a relationship between a CDM test and the ratios of the second resistance and the first resistance (see back ground of invention, p. 5, lines16-23).

5. Claims 5 and 6, the APA in view of Taillient disclose all limitations of claim 1. APA and Taillient do not disclose that a length of wiring connects the second clamping devices (113a)to the gate and the drain/source of the corresponding transistor (112a) is no more than 100 micrometers. However, It would have been obvious to one having ordinary skill in the art at the time invention was made to substitute a length of wiring to any desired values as long as it compatible with the requirements of the other components in the integrated circuit in order to minimize any resistance between its components. It has been held that

discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding to claim 7, APA discloses that the first resistance (R114) comprises a wiring resistance and contact resistance (see fig. 15).

Regarding to claims 8 and 9, APA discloses that the first resistance includes an effective channel resistance of an input path transistor (end to end path through the transistor 112a).

Regarding to claim 10, APA discloses that the second resistance (114a) comprises a supply potential wiring (118) and a contact resistance where the first and second clamping devices are connected to the supply potential wiring (118) (see fig. 18).

Regarding to claim 11, APA discloses that the semiconductor integrated circuit device (see fig. 18) comprises each first clamping device (111a) has a first terminal connected to one of the I/O terminal (110a), a second terminals of each first clamping device being connected to the second terminal (110b) of one of the the second clamping device (111b) by system wiring (118) of at least one supply terminal; and the second resistance (114a) comprises a contact resistance between the second terminal of the first clamping device and the supply potential wiring, a contact resistance between the second terminal of the second clamping device (113a).

Regarding to claims 12 and 13, APA discloses that each first clamping device (111a) has a first terminal connected to one of the I/O terminals (110a) and a second terminal connected to a first supply terminal (118) and each

second clamping device connected to a second supply terminal (117) different the first supply terminal.

6. Claims 14,19 and 20, APA in view of Taillient disclose all limitations of claim 1 except for each second clamping device selected from a group as claimed. As for the clamping device being various elements (an IGFET, an NPN bipolar, a diode, and a thyristor); it would have been obvious to one of ordinary skill in the art at the time the invention was made to select any known over-voltage protection element as deemed suitable in order to provide the over-voltage protection function. This is further demonstrated by applicant's various embodiments of the over-voltage protection as claimed absent persuasive evidence that particular type of over-voltage protection element is significant.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Li et. al. (U.S. Patent No. 5,477,414) disclose that the electrostatic discharge protection circuit can vary for transistor and not having to be the same depending on the level of protection required.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax

phone numbers for the organization where this application or proceeding is assigned are (703)-305-1341 for regular communications and (703)-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

D.N.
D.N.
September 30, 2002

9/30/02
KIM HUYNH
PRIMARY EXAMINER